

SEMICONDUCTOR STRUCTURE ON INSULATOR AND ITS MANUFACTURING METHOD

Patent Number: JP2098158

(3)

Publication date: 1990-04-10

Inventor(s): SATWINDER MALHI;; CHI-CHEONG SHEN;; SUNDARESAN RAVISHANKAR;; KENNETH E BEAN;; J MAC RAY ANDERSON;; GREG A GOPFFARTH;; JERRY D SMITH;; RICHARD E CLEY;; KEITH LINDBERG;; CHANG PENG-HENG

Applicant(s): TEXAS INSTR INC <TI>

Requested Patent: JP2098158

Application Number: JP19890154397 19890616

Priority Number(s):

IPC

Classification: H01L21/76; H01L21/306; H01L21/316; H01L21/331; H01L29/73

EC

Classification:

Equivalents:

Abstract

PURPOSE: To manufacture a substrate with no substantial dislocation at all by compensating strain by a method wherein, when an epitaxial layer is grown so as to bury a specific number of insulators as the substrates for LSI, the epitaxial layer is grown through the intermediary of a transposition compensating layer previously provided on the substrate.

CONSTITUTION: An each stopper alder 12 made of P<++> type Si lessening the transposition by doping with Ge is epitaxially grown on an N type or P type Si substrate 11 having 100 orientation so as to deposit an N type Si layer 13 on the layer 12 further to provide an N<++> type buried layer 14 if necessary. Next, a polycrystalline Si layer 16 is deposited on the buried layer 14 through the intermediary of an electric insulating layer 15 for thinning the substrate 1 side in the thickness of 2-4 mill by mechanical or ion grinding process. Successively, the remaining substrate 11 and the layer 12 positioned below the substrate 11 are etched away using a chemical so that a specific number of apertures may be bored in the exposed layer 13 to be filled up with insulators 30 such as SiC, SiO₂, etc., for the formation of a high quality substrate for LSI.

Data supplied from the esp@cenet database - I2